Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A linear scalable method for computing a Fast Fourier Transform (FFT) or Inverse Fast Fourier transform (IFFT) in a multiprocessing system using a decimation in time approach, comprising the steps of:

computing ~~first and second stages of $\log_2$N stages of~~ an N-point FFT/IFFT ~~as a single radix-4 butterfly operation while implementing the remaining ($\log_2$N-2) stages~~ using a first plurality of butterfly computational stages, each stage in the first plurality of stages employing a plurality of butterfly operations having a first radix, ~~using radix-2 butterfly operations, wherein each radix-2 butterfly operation employs a single radix-2~~ wherein each of the butterfly operations in each stage in the first plurality of stages has a single, un-nested computation loop of the first radix; ~~without employing nested loops;~~ and

distributing the plurality of butterfly operations in each stage of the first plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency in the stage.

2. (Currently Amended) A linear scalable method as claimed in claim 1 wherein said step of distributing butterfly operations in each stage is implemented by assigning to each processor of the multi-processor system respective addresses of memory locations corresponding to inputs and outputs required for each specific butterfly operation assigned to the processor.

3. (Currently Amended) A linear scalable system for computing a Fast Fourier Transform (FFT) or Inverse Fast Fourier transform (IFFT) in a multiprocessing system using a decimation in time approach, comprising:

means for computing a plurality of stages ~~first and second stages of $\log_2$N stages~~ of an N-point FFT/IFFT ~~as a single radix-4 butterfly operation while implementing the remaining ($\log_2$N-2) stages~~ using in each stage of the plurality of stages a plurality of ~~radix-2~~ butterfly operations, wherein each ~~radix-2~~ butterfly operation employs a single ~~radix-2~~ butterfly computation loop of a first radix and without employing nested loops; and

means for distributing the butterfly operations in each stage of the plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency in the stage.

4. (Original) A linear scalable system as claimed in claim 3 wherein said means for distributing the butterfly operations is implemented by means for assigning to each processor of the multi-processor system respective addresses of memory locations corresponding to inputs and outputs required for each specific butterfly operation assigned to the processor.

5. (Currently Amended) A computer program product comprising computer readable program code stored on a computer readable storage medium embodied therein for computing a Fast Fourier Transform (FFT) or Inverse Fast Fourier transform (IFFT) in a multiprocessing system using a decimation in time linear scalable approach, comprising:

computer readable program code means configured for computing ~~computing~~ first and second stages of $\log_2$N stages of an N-point FFT/IFFT as a single radix-4 butterfly operation while implementing the remaining ($\log_2$N-2) stages using radix-2 butterfly operations, wherein each radix-2 butterfly operation employs a single radix-2 butterfly computation loop without employing nested loops; and

computer readable program code means configured for distributing the butterfly operations in each stage such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency in the stage.

6. (Original) The computer program product as claimed in claim 5 wherein said computer readable program code means configured for distributing the butterfly operations is implemented by computer readable program code means configured for assigning to each processor of the multi-processor system respective addresses of memory locations corresponding to inputs and outputs required for each specific butterfly operation assigned to the processor.

7. (New) The method of claim 1 wherein the first radix is a radix-2 radix.

8. (New) The method of claim 7 wherein the first plurality of stages comprises N minus two stages, further comprising computing a first and second stage of $\log_2 N$ stages of the N-point FFT/IFFT as a single radix-4 butterfly operation.

9. (New) The method of claim 1 wherein the first plurality of stages comprises N stages.

10. (New) The method of claim 1 wherein an output of a last stage in the first plurality of stages provides the computed N-point FFT/IFFT.

11. (New) The method of claim 2, wherein the assigning addresses to each processor comprises inserting a binary digit in an address of a memory location.

12. (New) The system of claim 3 wherein the first radix is a radix-2 radix.

13. (New) The system of claim 12 wherein the plurality of stages comprises N minus two stages, further comprising computing a first and second stage of $\log_2 N$ stages of the N-point FFT/IFFT as a single radix-4 butterfly operation.

14. (New) The system of claim 3 wherein the first plurality of stages comprises N stages.

15. (New) The system of claim 4 wherein the means for assigning is configured to insert a binary digit in an address of a memory location.

16. (New) A computer-readable memory medium whose contents cause a system having a plurality of processors to perform a linear scalable method, the method comprising:

computing an N-point FFT/IFFT using a first plurality of butterfly computational stages, each stage in the first plurality of stages employing a plurality of butterfly operations having a first radix, wherein each of the butterfly operations in each stage of the first plurality of stages has a single, un-nested computation loop of the first radix; and

distributing the plurality of butterfly operations in each stage of the first plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency in the stage.

17. (New) The computer-readable memory medium of claim 16 wherein the distributing butterfly operations in each stage comprises assigning to each processor of the multi-processor system respective addresses of memory locations corresponding to inputs and outputs required for each specific butterfly operation assigned to the processor.

18. (New) The computer-readable memory medium of claim 17 wherein the assigning addresses to each processor comprises inserting a binary digit in an address of a memory location.

19. (New) The computer-readable memory medium of claim 16 wherein the first plurality of stages comprises N stages.

20. (New) The computer-readable memory medium of claim 16 wherein an output of a last stage in the first plurality of stages provides the computed N-point FFT/IFFT.